Amendments to the Claims

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently amended) An algorithmic analog-to-digital converter (ADC) comprising:

a sample-and-hold circuit clocked by a sampling clock having a substantially uniform clock period; and

an ADC processing unit clocked by ~~an~~ a single internal ADC clock having at least two available cycles per sampling clock period, wherein at least one of the available cycles in the single internal ADC clock comprises a length different than a length of at least one of the other cycles in the single internal ADC clock.

2. (Currently amended) An algorithmic ADC as claimed in claim 1, wherein the single internal ADC clock has at least one longer cycle producing a more accurate conversion and at least one shorter cycle producing a less accurate conversion.

3. (Currently amended) An algorithmic ~~ADC as claimed in claim 1, and further~~ analog-to-digital converter (ADC) comprising:

a sample-and-hold circuit clocked by a sampling clock having a substantially uniform clock period;

an ADC processing unit clocked by an internal ADC clock having at least two available cycles per sampling clock period, wherein at least one of the available cycles comprises a length different than a length of at least one of the other cycles; and

a DLL comprised of at least two delay elements having differing amounts of delay that are used to generate the internal ADC clock.

4. (Canceled)

5. (Currently amended) An algorithmic ~~ADC as claimed in claim 4,~~ analog-to-digital converter (ADC) comprising:

a sample-and-hold circuit clocked by a sampling clock having a substantially uniform clock period; and

an ADC processing unit clocked by an internal ADC clock having at least two available cycles per sampling clock period, wherein at least one of the available cycles comprises a length different than a length of at least one of the other cycles,

wherein the ADC processing unit comprises a multiplying digital-to-analog converter (MDAC) and a sub-ADC, and

wherein the sample-and-hold circuit is integrated with the MDAC.

6. (Original) An algorithmic ADC as claimed in claim 5, wherein each internal ADC clock cycle is further sub-divided into at least two phases, wherein during at least one phase switchable capacitors are coupled to a residue or sampled voltage provided by the MDAC. and during one other phase the capacitors are coupled to a reference voltage.

7. (Original) A video encoder chip comprising an algorithmic ADC as claimed in claim 1.

8. (Original) A video decoder chip comprising an algorithmic ADC as claimed in claim 1.

9. (Original) A set top box comprising an algorithmic ADC as claimed in claim 1.

10. (Currently amended) An electronic ~~applicance~~ appliance comprising an algorithmic ADC as claimed in claim 1.

11. (Currently amended) A method for converting an input analog signal to an output digital bit stream, comprising:

sampling and holding the input analog signal during a sampling clock period;

generating at least two bits using an algorithmic ADC unit clocked by ~~an~~ a single internal ADC clock having at least two cycles of variable length per sampling clock period.

12. (Currently amended) A method as claimed in claim 11, wherein the single internal ADC clock has at least one longer cycle producing a more accurate conversion and at least one shorter cycle producing a less accurate conversion.

13. (Currently amended) A method ~~as claimed in claim 11, and further~~ for converting an input analog signal to an output digital bit stream comprising:

sampling and holding the input analog signal during a sampling clock period;

generating at least two bits using an algorithmic ADC unit clocked by an internal ADC clock having at least two cycles of variable length per sampling clock period; and

generating the internal ADC clock using a DLL comprised of delay elements having differing amounts of delay.

14. (Currently amended) A method for reducing the conversion time of an algorithmic ADC comprising:

providing ~~an~~ a single internal ADC clock having ~~a variable clock period~~ at least two cycles of different lengths.

15. (Currently amended) A method as claimed in claim 14, wherein the single internal ADC clock has cycles that are longer during operational phases proximate the MSB resolution and cycles that are shorter during operational phases proximate the LSB resolution.

16. (Currently amended) A clock generation system for an algorithmic ADC comprising:

means for generating a sampling clock; and

means for generating an internal ADC clock having N cycles per sampling clack period, the cycles having variable length and being longer during operational phases proximate the MSB resolution and shorter during operational phases proximate the LSB resolution, wherein the means for generating an internal ADC clock comprises a DLL comprised of delay elements having differing amounts of delay.

17. (Canceled)

18. (Currently amended) A method for converting an input analog signal to an output digital bit stream, comprising:

a step for sampling and holding the input analog signal during a sampling clock period;

a step for generating ~~an~~ a single ADC clock having N cycles of variable length per sampling clock period, wherein at least one cycle within the single ADC clock has a different length than another cycle within the single ADC clock;

a step for generating an intermediate analog voltage per cycle using the sampled analog signal and residue voltages derived from the sampled analog signal;

a step for generating a set of data bits per cycle from the intermediate analog voltage;

a step for generating feedback signals for generating the intermediate analog voltage in the next cycle; and

a step for generating the output digital bit stream using the N sets of data bits.

19. (Original) A method as claimed in claim 18, wherein each cycle is further divided into two phases, and wherein during a first phase a sampled analog signal or residue voltage is applied to switched capacitors, and wherein during a second phase reference voltages are applied to the switched capacitors.

20. (Original) A method as claimed in claim 19, wherein the feedback signals determine what reference voltages are applied to the switched capacitors.

21. (Original) A method as claimed in claim 18, wherein the ADC clock has longer cycles during operational phases requiring more accuracy and shorter cycles during operational phases requiring less accuracy.